

Total No. of Questions : 12]

SEAT No. :

[Total No. of Pages : 4

P3143

B.E. (Semester - II)
COMPUTER
Advanced Computer Architecture
(2008 Pattern)

Time : 3 Hours]

[Max. Marks : 100

Instructions to the candidates:

- 1) *Answers to the two sections should be written in separate answer books.*
- 2) *Answer any three questions from each section.*
- 3) *Neat diagrams must be drawn wherever necessary.*
- 4) *Figures to the right side indicate full marks.*
- 5) *Use of Calculator is allowed.*
- 6) *Assume suitable data if necessary.*

SECTION - I

- Q1)** a) What do you mean by Coarse grain parallelism and Fine grain parallelism? With examples of each category, explain how Multitasking OS achieves parallelism? **[10]**
- b) Prove that 'n' stage pipeline processor can be at most 'n' times faster than a corresponding non-pipelined serial processor. **[8]**

OR

- Q2)** a) Discuss the different ways of classifying the parallel computing systems. **[10]**
- b) State and explain Explicitly Parallel Instruction computing (EPIC) Features. **[8]**

P.T.O.

Q3) a) Consider the following pipe line reservation table : **[10]**

	0	1	2	3	4	5	6
S1	X		X				X
S2				X		X	
S3			X		X		

- i) Determine latencies in the forbidden list F and Collision vector C.
 - ii) Draw the state transition diagram.
 - iii) List all simple cycles and greedy cycles.
 - iv) Determine minimum constant latency and minimum average latency.
 - v) Let the pipeline clock period be $\tau = 20$ ns. Determine the maximum throughput of the pipeline.
- b) Explain the following terms with respect to pipeline processors . **[6]**
- i) Hazards
 - ii) Internal Forwarding

OR

- Q4) a)** With the help of suitable flowchart / diagram explain in detail branch prediction logic implemented in Pentium architecture. **[8]**
- b) What is meant by pipeline, superscalar and super pipeline processor? What are the various factors placing constraints on new start of pipeline processes? **[8]**
- Q5) a)** With suitable example, discuss the efficiency of vector processing over scalar processing. **[8]**
- b) Draw a 3-cube n/w as multistage network. State and obtain the permutation cycles for all the routing functions. **[8]**

OR

Q6) a) Discuss characteristics of vector processors. Explain implementation of following loop in conventional scalar processor and vector processor. [8]

DO 100 I = 1, N

$$A(I) = B(I) + C(I)$$

$$100 B(I) = 2 * A(I+1)$$

b) Explain following pipelined vector processing methods with respect to vector summation computation. [8]

i) Vertical Processing

ii) Vector Looping

How intermediate results are handled in both the cases?

SECTION - II

Q7) a) What are the cache write policies used for cache updating? With state diagram explain the Write Once cache coherency protocol. [9]

b) List different dynamic priority arbitration algorithms used in bus based multi-processor systems and discuss any 2 such algorithms in brief. [9]

OR

Q8) a) Compare the shared memory system architecture with distributed systems. What are the desirable processor characteristics used in multi-processor systems? [9]

b) With neat diagram explain the design of crossbar switch. Compare the crossbar switch Interconnection Network with multi-ported memory model. [9]

Q9) a) What are multi-threaded architectures? Discuss the various performance parameters of multi-threaded processor architectures. [8]

b) Compare between synchronous and asynchronous message passing. [8]

OR

Q10) a) What is latency hiding? Explain any Two methods used for Latency Hiding in multi-threaded architectures. [8]

b) With example explain message passing parallel programming. What is SPMD Programming? [8]

Q11) a) Explain following communication functions used in MPI [8]

i) MPI_Scatter()

ii) MPI_Gather()

iii) MPI_Bcast()

iv) MPI_Allgather()

b) With standard functions discuss how message passing is facilitated in PVM. [8]

OR

Q12) a) With standard constructs discuss the important features of CCC parallel programming language. [8]

b) Compare between synchronous and Asynchronous parallel algorithms for multiprocessor systems and discuss standard primitives used. [8]

